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A 143 dB Delta-Sigma Modulator for Biomedical Applications

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Abstract

This paper presents a single loop fourth-order delta-sigma modulator topology of cascade of integrator with multiple feedback (CIFB) having 3-bit quantizer. The number of levels in the quantizer increased for higher performance. The modulator noise transfer function (NTF) and signal transfer function (STF) exploited for higher performance. The out-of-band gain (OBG) of 1.5 selected considering the stability of higher order modulator. The high oversampling ratio (OSR) considered for small bandwidth applications. The maximum quantization noise is suppressed by NTF zeroes optimization. A full-scale signal of the modulator is 0.55-V considering the higher order loop filter stability. Due to CIFB topology, there is no peaking in the STF while STF response is flat. The zeroes of the NTF are optimized for maximum quantization noise and poles are adjusted inside the unit circle. The complete modulator loop filter has four integrators in the loop filter with multiple feedback digital-to-analog converter (DAC) for maximum stability. The complete modulator simulation shows it can achieve signal-to-noise-ratio (SNR) of 143 dB with oversampling ratio (OSR) of 128.

Keywords: CIFB; DAC; Loop filter; Noise Transfer Function; OBG; Signal Transfer Function

1. Introduction

The growing health concerns demands the development of biomedical devices. The biosensor for neural spikes, electroencephalography (EEG), electrocardiography (ECG), electromyography (EMG). The analog-to-digital (ADC) used for digitizing the front-end analog signal. The portable health systems either wireless or wired devices requires battery. The use of battery powered biomedical devices increases the requirement for low power circuit techniques. The design of low-power circuit can reduce the number of battery cells for low weight and small system size. At the same time, low power circuit design can increase the operation time for biomedical application. The delta-sigma modulator has become a usual technique for ADC conversion. This is due to reason delta-sigma modulator circuits are structured simply with low-accuracy

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analog parts and very suitable in low frequency, high performance, and low power application. The single-bit modulators are simple and easy to implement but have limited performance.

To enhance the performance of the modulator, the number of integrators in the loop filter increase while the number of levels in the quantizer also raised to meet the performance requirements [1]. A delta-sigma modulator design for biomedical sensor application with power dissipation of 540 nW. It presents an extremely low-power delta-sigma modulator for battery-powered biomedical sensors. Distributed feed-forward architecture is used to achieve efficient operation at a supply voltage of 0.6 V. To achieve a wide input range in this low voltage environment, the bulk-driven operational transconductance amplifier is designed with a self-cascode output stage. The modulator has a dynamic range of 52 dB with only 540 nW of power for the 250-Hz bandwidth. Such a significant reduction in power consumption allows diverse battery powered biomedical applications that have limited battery power, such as the electro-oculogram, electroencephalogram, and electrocardiogram [2].

The recorded neural data are frequently corrupted by large amplitude artifacts that are triggered by a variety of sources, such as subject movements, organ motions, electromagnetic interferences, and discharges at the electrode surface. To prevent the system from saturating and the electronics from malfunctioning due to these large artifacts, a wide dynamic range for data acquisition is demanded, which is quite challenging to achieve and would require excessive circuit area and power for implementation.

In this paper, we present a high-performance delta-sigma modulator along with several design techniques and enabling blocks to reduce circuit area and power. The modulator was fabricated in a 0.18-µm CMOS process. Powered by a 1.0-V supply, the chip can achieve an 85-dB peak signal-to-noise-and-distortion ratio (SNDR) and an 87-dB dynamic range when integrated over a 10-kHz bandwidth. The total power consumption of the modulator is 13 µW, which corresponds to a figure-of-merit (FOM) of 45 fJ/conversion step. These competitive circuit specifications make this design a good candidate for building high precision neuro sensors [3].

A second-order asynchronous delta-sigma modulator (ADSM) is proposed based on the active-RC integrators. The ADSM is implemented in the 0.18 µm CMOS Logic or Mixed-Signal/RF, General Purpose process from the Taiwan Semiconductor Manufacturing Company with a center frequency of 848 kHz at a supply voltage of 1 V with a 92 dB peak signal-to-noise and distortion ratio (SNDR), which corresponds to 15- bit resolution. These parameters were achieved in all the endogenous bioelectric signals bandwidth of 10 kHz. The ADSM dissipated 295 µW and had an area of 0.54 mm^2.

Table I : CIFB Topology Cofficients

Parameters	Values
a1	0.006
a2	0.064
a3	0.308
a4	0.805
g1	.007e-3
g2	.447e-3
b1	0.006
c1	1
c2	1
c3	1
c4	1

Table II: Modulator performance

OSR	SNR
8	22
16	56
32	86
64	112
128	143

Table III: Modulator performance

OBG	SNR
1.5	143
1.6	148
1.7	154
1.8	155
1.9	158
2	159
2.1	163
2.2	162
2.3	163
2.4	166
2.5	166.5
2.7	169
2.8	169.9
3.5	175.8
4	176.6
4.5	177

Table IV : Full-Scale

Input Signal	SNR
.55	143
0.6	144
0.65	148
0.7	146
0.75	142

The proposed ADSM with a high resolution, wide bandwidth, and rail-to-rail input voltage range provides the universal solution for endogenous bioelectric signal processing [4]. A sub-μW power consumption delta-sigma modulator with a target 10-bit resolution for biomedical application. A fully passive loop filter based CTDSM was first realized followed by a digital comb LPF and decimator. The loop filter employs an asynchronous NRZ DAC and a feedforward summing enabled comparator realization.

We propose a low power architectural implementation of a digital comb filter. The low power operation is enabled at the architectural level due to the novel clock enabled adder-based comb filter. Further, a proposed pass gate and keeper based full adder circuit implementation is used for sub-μW power consumption. The design was realized in a standard 180 nm CMOS mixed mode technology in Semiconductor Laboratory (SCL), India. Simulation results show a power consumption of 920 nW for the ΔΣ ADC for a 10 kHz biomedical bandwidth [5].

This paper presents a fourth-order three-bit CIFB delta-sigma modulator modeled, and simulation shows it can achieve higher SNR of 143 dB. The number of levels in the quantizer increased for higher performance. The modulator noise transfer function (NTF) and signal transfer function (STF) exploited for higher performance. The out-of-band gain (OBG) of 1.5 selected considering the stability of higher order modulator. The high oversampling ratio (OSR) considered for small bandwidth applications. The maximum quantization noise is suppressed by NTF zeroes optimization.

A full-scale signal of the modulator is 0.55-V considering the higher order loop filter stability. Due to CIFB topology, there is no peaking in the STF while STF response is flat. The zeroes of the NTF are optimized for maximum quantization noise and poles are putted inside the unit circle. The complete modulator loop filter has four integrators in the loop filter with multiple feedback digital-to-analog converter (DAC) for maximum stability. The complete modulator simulation shows it can achieve signal-to-noise-ratio (SNR) of 143 dB with oversampling ratio (OSR) of 128.

After the introduction, the second section discusses the design of the modulator with CIFF topology, while the third section describes the modeling and simulation of the modulator and explain the operation of the second-order single bit. Finally, the section four concludes the paper.

Modulator Design

A fourth-order modulator with CIFB topology and multi-bit quantization is modeled using Delta-Sigma Toolbox [6]. Due to CIFB topology the signal-transfer-function (STF) will not have any peaking issues but requires high power operational amplifier. It can be used for integrator as the signal swing inside the loop filter is large due to multiple feedback paths. The CIFB fourth-order modulator with NTF zero optimization technique can achieve signal-to-noise ratio of 143 dB with OSR of 128 with an OBG of 1.5. The modulator with CIFB topology coefficients is obtained from the Delta-Sigma Toolbox [6] shown in Table-I.

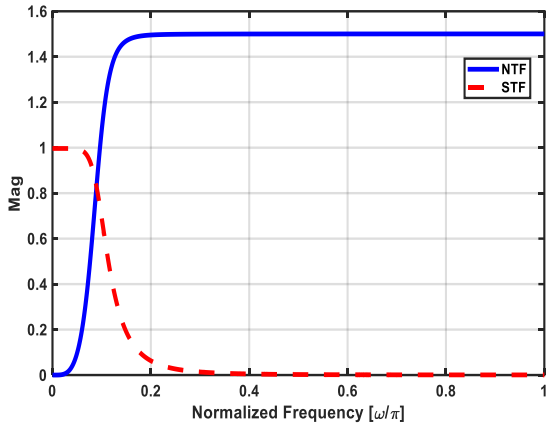

Figure 1: STF and NTF plot (CRFB)

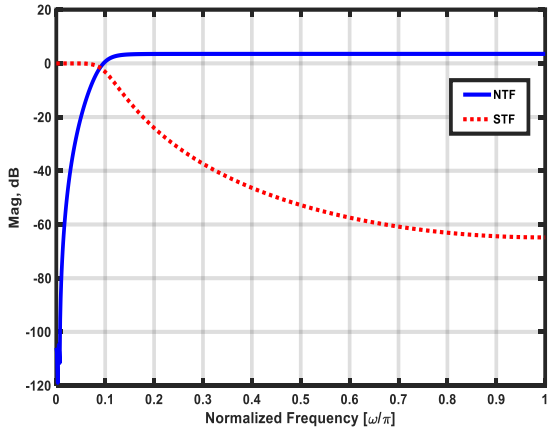

Figure 2: STF and NTF plot (CRFB)

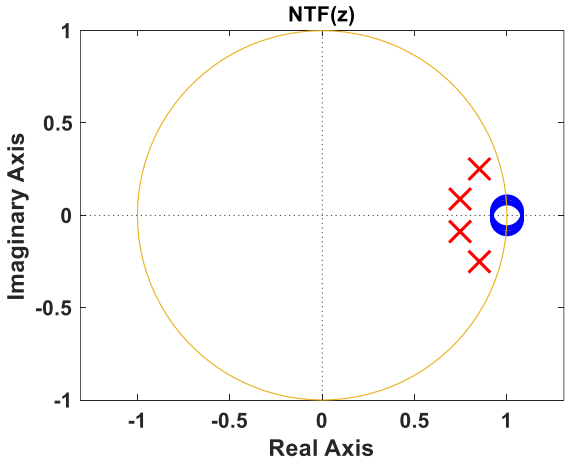

Figure 3: Unit Circle

The modulator feedback coefficients are a_1, a_2, a_3, a_4. While c_1, c_2, c_3, c_4, is the interstage coefficient. The NTF zero optimization technique is implemented using g_1 and g_2 coefficients.

The Table II shows the OSR versus SNR comparison, to consider different bandwidth. It is shown clearly that higher OSR will results in increased SNR. The out-of-band Gain (OBG) is very important for consideration of high performance of the modulator. The Table-III shows the effect of lower OBG and higher OBG with low to high SNR performance. The Figure 1 shows the NTF and STF plot with OBG of 1.5. The STF clearly shows without any peaking effect with low-pass filter response as the modulator is low-pass. While the NTF shows the high pass filter response. Which shows the quantization noise attenuation at the low frequencies. The Table IV shows the different input signal values, which shows different performance values for different input signal. The Figure 2 also shows the STF and NTF plot performance in dB. The Figure 3 shows the poles and zeroes plot at unit circle in z-domain. The poles lies inside the unit circle, while the zeroes at the DC. Due to the CIFB topology the signal swing inside the loop filter is higher, this effect can be observed in Figure 4. Figure 5 shows the output power spectral density (PSD).

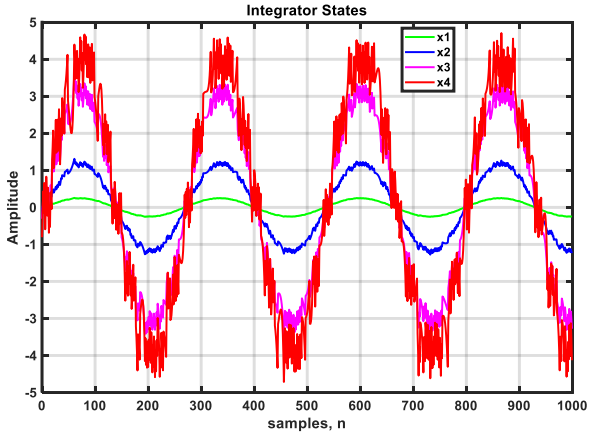

Figure 4: Output PSD plot (CRFB)

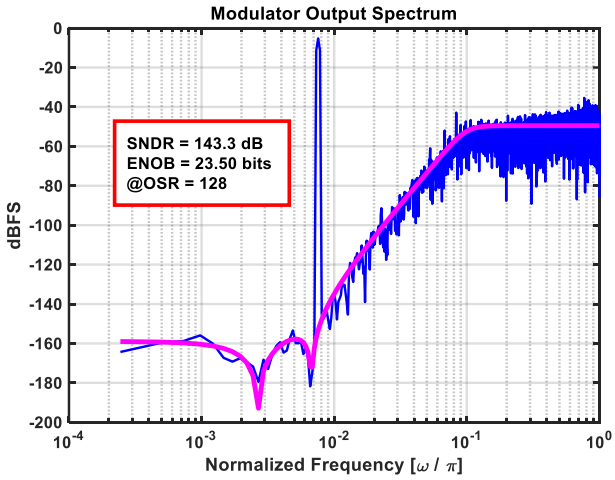

Figure 5: Output PSD plot (CRFB)

Table V : State-of-The-Art Comparsion

	Ref[4]	Ref[8]	This work
Technology	180nm	130nm	Simulation
Topology	ADSM	DTDSM	DTDSM
Resolution	15-bit	13-bit	23-bit
Order	2	3	4
Quantizer	1-Bit	1-bit	3-Bit
Bandwidth	10 kHz	20 kHz	10 kHz
SNR	92 dB	76 dB	143 dB
Dynamic Range	112 dB	82 dB	143 dB

Results & Discussion

The simulation shows that the proposed fourth-order modulator can achieve 143-dB SNR for input signal of 0.55-V. Due to the higher order modulator, moderate full scale of 0.55-V selected. For higher values of input signal, much higher resolution can be achieved. The operational amplifiers inside all the integrators are ideal, so there is no DC gain limitation, also no slew-rate limit. The 3-bit quantizer and DAC is also ideal. The 3-bit quantizer means 8 levels. So the DAC mismatch can also degrade the performance, which is avoided in this case to get an estimate of the performance. The modulator noise transfer function (NTF) and signal transfer function (STF) exploited for higher performance. The out-of-band gain (OBG) of 1.5 selected considering the stability of higher order modulator. The switch non-linearity non-ideality also avoided understanding the modulator behavior for high performance. Table-V shows the State-of-The-Art comparison with simulation and also circuit results. The proposed modulator only simulated, and results are provided.

2. Conclusion

A fourth-order three-bit CIFB delta-sigma modulator modeled, and simulation shows it can achieve higher SNR of 143 dB. The number of levels in the quantizer increased for higher performance. The high oversampling ratio (OSR) considered for small bandwidth applications. The maximum quantization noise is suppressed by NTF zeroes optimization. A full-scale signal of the modulator is 0.55-V considering the higher order loop filter stability. Due to CIFB topology, there is no peaking in the STF while STF response is flat. The zeroes of the NTF are optimized for maximum quantization noise and poles are putted inside the unit circle. The complete modulator loop filter has four integrators in the loop filter with multiple feedback digital-to-analog converter (DAC) for maximum stability. The complete modulator simulation shows it can achieve signal-to-noise-ratio (SNR) of 143 dB with oversampling ratio (OSR) of 128.

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3. References

[1] S. Norsworthy, Richard Schreier, G.C. Temes, Delta-Sigma Data Converter Theory, Design, and Simulation, John Wiley & Sons, Inc., Hoboken, New Jersey, 1997.

[2] Yoon Younghyun, Roh Hyungdong, Lee Hyuntae, Roh Jeongjin, A 0.6-V 540-nW Delta-Sigma Modulator for Biomedical Sensors, Analog Integr Circ Sig Process, **75,** 323-327 (2013).

[3] Xu Hian, Zhao Menglian, Wu Xiaobo, Islam Md. Kafiul, Yang Zhi, A High Performance Delta-Sigma Modulator for Neurosensing, Journal of sensors MDPI, **15(8),** 19466-19486 (2015).

[4] Kledrowetz Vilem, Fujcik Lukas, Prokop Romn and Haze Jiri, A 1-V 92 dB SNR 10 kHz Bandwidth Second-Order Asynchronous Delta-Sigma Modulator for Biomedical Signal Processing, Journal of sensor MDPI, 4137, 2020.

[5] Somappa Laxmeesha, Baghini Maryam Shojaei, A Sub-uW Power 10 Bit Delta-Sigma ADC for Biomedical Applications, IEEE 63rd International Midwest Symposium on Circuit and Systems (MWSCAS), 09-12 August. 2020.

[6] R. Scherier Delta-Sigma Toolbox ((http://www.mathworks.com/matlancentral/fileexchange/19-delta-sigma-toolbox).

[7] S. Brigati SDToolbox (http://www.mathworks.com/matlabcentral/fileexchange/2460-sd-toolbox).

[8] Yoon, Y.; Choi, D.; Roh,J, A 0.4 V 63 µW 76.1 dB SNDR 20kHz Bandwidth Delta-Sigma Modulator Using a Hybrid Switching Integrator, IEEE Journal Solid-State Circuit **50,** 234-235 (2015).